Shoubra Faculty of Engineering

Model No.12
Course Specifications : test - (5779)
(2014-2015)

Faculty : Shoubra Faculty of Engineering

Department : Electrical Engineering Department

1- Course Data

Course Code : ECE324C Course Title : test - (5779) Study Year : Third Year
Specialization :
Teaching Hours:
Lecture : Tutorial : 4 Practical : 4

2- Course Aim

For students undertaking this course, the aims are to:

2.1 gain an experimental experience in designing logic circuits
2.2 gain an experimental experience in using the VHDL simulation language.

3- Intended Learning Outcomes of Course (ILOS)

a- Knowledge and Understanding

On completing this course, students will be able to:

a-1 Identify the Principles of electrical waves and signals and design electronic circuits using different components related to logic circuits. (a4)
a-2 List the Methodologies of solving logic circuits problems and simulate circuits using VHDL language and a simulator . (a5)
a-3 Broad general education necessary to understand the impact of logic circuits solutions in a global and societal context (a18)

b- Intellectual Skills

At the end of this course, the students will be able to:

b-1 Select appropriate mathematical and logical computer-based methods for modeling and analyzing problems related to logic circuits. (b1)

b-2 Think in a creative and innovative way in problem solving and design of logic circuits. (b3)

b-3 Combine, exchange, and assess different ideas, views, and knowledge from a range of practical sources in the field of logic circuits.(b4)

b-4 -Select, synthesize, and apply suitable IT tools to logic circuits problems.(b14)

c- Professional Skills

On completing this course, the students are expected to be able to:

c- 1 Apply knowledge of mathematics, waves, design, business context and engineering practice to logic circuits problems. (c1)

c- 2 Professionally merge the electronics knowledge, understanding, and feedback to improve design, product and services in the field of logic circuits.(c2)

c- 3 Create or re-design a system, and carry out specialized electronic circuits designs. (c3)

c- 4 Write computer programs using VHDL language on professional levels achieving acceptable quality measures in software development in field of logic circuits.(c14)

c-5 Use appropriate specialized simulators, computational tools and packages.(c15)

d- General Skills

At the end of this course, the students will be able to:

d- 1 Collaborate effectively within multidisciplinary team. (d1)

d- 2 Work in stressful environment and within constraints. (d2)

d- 3 Communicate effectively (d3)

d- 4 Demonstrate efficient IT capabilities. (d4)

d- 5 Lead and motivate individuals. (d5)

d- 6 Refer to relevant literatures. (d9)

4- Course Contents

No.	Topics	No. of hours
1	Logic Circuits – AND/OR	8
2	2 inpute OR -> 3 input OR,INVERTER	8

3	TIMING Diagrams investigation	8
4	DeMORGANS'S LAW CASE , NAND-NOR-XOR	8
5	BINARY HALF/FULL ADDER	16
6	FLIP FLOPS-	8
7	SHIFT REGISTERS	8
8	VHDL	40

5- Teaching and Learning Methods

5.1- Modified Lectures
5.2- Practical training / laboratory
5.3- Seminar / workshop
5.4- Class activity
5.5- Case study
5.6- Assignments / homework

6- Teaching and Learning Methods of Disables

6.1- None

7- Student Assessment

a- Student Assessment Methods

1	Assignments to assess knowledge and intellectual skills.
2	Quizzes to assess knowledge, intellectual and professional skills.
3	Mid-term exam to assess knowledge, intellectual, professional and general skills.
4	Final exam to assess knowledge, intellectual, professional and general skills.

b- Assessment Schedule

No.	Assessment	Week
1	Assignments	2,5,9,11
2	Quizzes	4,6,10,12
3	Mid-term exam	8
4	Final exam	15

c- Weighting of Assessments

Assessment	Weight
Mid_Term Examination	15 %
Final_Term Examination	50 %
Oral Examination	20 %
Practical Examination	0 %
Semester work	5 %
Other types of assessment	10 %
Total	100 %

8- List of References

a- Course Notes

1- Course notes prepared by instructor.

b- Books

1- Peter J. Ashenden - The Designer’s Guide to VHDL, Third Edition - 2008

c- Recommended Books

1- The Manual associated with the lab kit

- Course Coordinator : Dr/May Ahmed Salama Mohamed

- Head of Department : Prof/ Sayed Abo-Elsood Sayed Ward

Shoubra Faculty of Engineering

Model No.12
Course Specifications : test - (5779)
(2012-2013)

University : Benha university

Faculty : Shoubra Faculty of Engineering

Department : Electrical Engineering Department

Matrix of Knowledge and Skills of the course

No.	Topics	week	Basic Knowledge	Intellectual Skills	Professional Skills	General Skills
1	Logic Circuits – AND/OR	2	a1	b1	c3,c5	d1,d2,d6
2	2 inpute OR -> 3 input OR,INVERTER	2	a2	b1,b2,	c2,c3,c4	d1,d2,d6
3	TIMING Diagrams investigation	2	a1,a3	b2,b3,b4	c3,c5	d1,d2,d3,d6
4	DeMORGANS' S LAW CASE , NAND-NOR-XOR	2	a1,a2	b2,b3,b4	c1,c2,c3,c4	d1,d2,d6
5	BINARY HALF/FULL ADDER	2	a1,a3	b2,b4	c3,c5	d1,d2,d6
6	BINARY	2	a1,a3	b1,b2,b3,b4	c2,c3,c5	d1,d2,,d3d6

	HALF/FULL SUBTRACTER					
7	FLIP FLOPS-	2	a2,a3	b1,b2,b3	c2,c3,c4	d1,d2,d6
8	Midterm	2	a2,a3	b1,b3,b4	c2,c3,c5	d1,d2,d6
9	SHIFT REGISTERS	2	a1,a2	b1,b2,b3,b4	c2,c3,c4,c5	d1,d2,d3,d6
10	VHDL	2	a2,a3	b3,b4	c2,c3,c4	d1,d2,d6,d4,d5
11	VHDL	2	a1,a3	b4	c2,c3,c5	d1,d2,d6,d4,d5
12	VHDL	2	a2,a3	b2,b3,b4	c2,c3,c4,c5	d1,d2,d6,d4,d5
13	VHDL	2	a1,a2	b2,b4	c2,c3,c5	d1,d2,d6,d4,d5
14	VHDL		a1,a2	b2,b4	c3,c5	d1,d2,d6,d4,d5
15	Final Exam		a2,a3	b1,b2,b3,b4	c2,c3,c5	d1,d2,d6

Matrix of course content and ILO's

Course Title: test - (5779) **Code**: ECE324C **Lecture**:- **Tutorial** : 4 **Practical**: 4 **Total:** 8
Program on which the course is given: M.Sc. Electrical Engineering (Computer Engineering)
Major or minor element of program: Major
Department offering the program: Electrical Engineering Department
Department offering the course: Electrical Engineering Department
Academic year / level: 2012-2013 second semester
Date of specifications approval: 20/6/2010

Course content	a1	a2	a3	b1	b2	b3	b4	c1	c2	c3	c4	c5	d1	d2	d3	d4	d5	d6
Logic Circuits – AND/OR	✓			✓						✓		✓	✓	✓				✓
2 inpute OR -> 3 input OR,INVERTER		✓		✓	✓				✓	✓	✓		✓	✓				✓
TIMING Diagrams investigation	✓		✓		✓	✓	✓			✓		✓	✓	✓	✓			✓
DeMORGANS'S LAW CASE , NAND-NOR-XOR	✓	✓			✓	✓	✓	✓	✓	✓	✓		✓	✓				✓
BINARY HALF/FULL ADDER	✓		✓		✓		✓			✓		✓	✓	✓				✓
FLIP FLOPS		✓	✓	✓	✓	✓			✓	✓	✓		✓	✓				✓
SHIFT REGISTERS	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓			✓
VHDL	✓	✓			✓		✓			✓		✓	✓	✓		✓	✓	✓

Matrix of course aims and ILO's

Course Title: test - (5779) **Code**: ECE324C **Lecture**:- **Tutorial** : 4 **Practical**: 4 **Total:** 8
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Course content	a1	a2	a3	b1	b2	b3	b4	c1	c2	c3	c4	c5	d1	d2	d3	d4	d5	d6
gain an experimental experience in designing logic circuits	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	

- course ILOS VS Program ILOS:

	A4	A5	A18	B1	B3	B4	B14	C1	C2	C3	C14	C15	D1	D2	D3	D4	D5	D9
A1	√																	
A2		√																
A3			√															
B1				√														
B2					√													
B3						√												
B4							√											
C1								√										
C2									√									
C3										√								
C4											√							
C5												√						
D1													√					
D2														√				
D3															√			
D4																√		
D5																	√	
D6																		√

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