Benha University
Faculty of Engineering at Shoubra
Electrical Engineering Department
M.Sc. (Electronics Engineering)

Final Term Exam (Spring 2015)
Date: Tuesday (2/6/2015)
Subject: CAD
Duration: 3 hours (for the 2 parts)

Part (II)

Answer all the following questions in the same sheet

- **No. of questions : 3**
- **Total Mark: 70 Marks**

Model Answer

Question (1) (20 Marks)

1- Mention some of the electronic design objectives.
2- List some challenges to the design process. Give some possible solutions.
3- Discuss the abstraction hierarchy design paradigm.
4- What is the aim of testing? What are the advantage of Built-In Self Test (BIST).

Answer of Question (1)

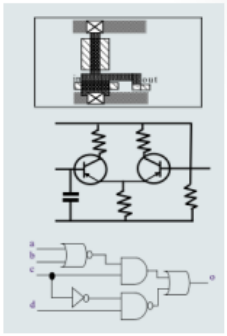
1. Objectives:
   - Unit cost: the cost of manufacturing each copy of the system, excluding NRE cost.
   - NRE cost (Non-Recurring Engineering cost): The one-time cost of designing the system.
   - Size: the physical space required by the system.
   - Performance: the execution time or throughput .
   - Power: the amount of power consumed by the system.
   - Testability: the easiness of testing the system to make sure that it works correctly.
   - Flexibility: the ability to change the functionality of the system without incurring heavy NRE cost.
2. Challenges:
   - System complexity
   - Increasing functionality and diversity
   - Increasing performance
   - Stringent design requirements
   - Low cost and low power
   - Dependability: reliability, safety and security
   - Testability and flexibility
   - Technology challenges for cost-efficient implementation
   - Deep submicron effects (e.g., cross talk and soft errors)

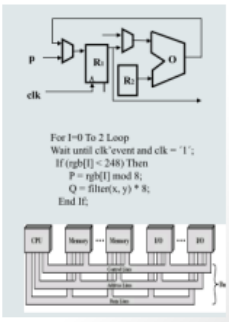
   Possible Solutions:
   - Powerful design methodology and CAD tools.
   - Advanced architecture (modularity).
   - Extensive design reuse.

3. Abstraction hierarchy:

Abstraction Hierarchy

- **Layout/silicon level** : The physical layout of the integrated circuits is described.
- **Circuit level** : The detailed circuits of transistors, resistors, and capacitors are described.
- **Logic (gate) level** : The design is given as gates and their interconnections.
- **Register-transfer level (RTL)** : Operations are described as transfers of values between registers.
- **Algorithmic level** : A system is described as a set of usually concurrent algorithms.
- **System level** : A system is described as a set of processors and communication channels.





4. Testing aim:

Testing aims at the detection of physical faults (production errors/defects and physical failures).

Advantages of BIST:

- No need for expensive ATE.
- Speed testing.
- Concurrent test possible.
- Support field test and diagnosis

Question (2) (15 Marks)

1- Give some applications of the Hardware Description Language (HDL).
2- What is the difference between behavioral and structural ways in VHDL modeling?
3- Describe a test bench model.

Answer of Question (2)

5. HDL Applications
    - Model and document digital systems
        - Different levels of abstraction e.g. behavioral, structural, etc.
    - Verify design
    - Synthesize circuits
        - Convert from higher abstraction levels to lower abstraction levels
6. Behavioral & Structural ways

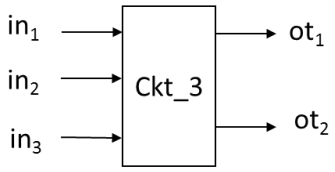
Behavioral ways	Structural way:

• *Architecture body*
  ○ describes an implementation of an entity
  ○ may be several per entity
• *Behavioral* architecture
  ○ describes the algorithm performed by the module
  ○ contains
  ▪ *process statements*, each containing
  • *sequential statements*, including
  ○ *signal assignment statements* and
  ○ *wait statements*
	• implements the module as a composition of subsystems
	• contains
	  • *signal declarations*, for internal interconnections
	  • the entity ports are also treated as signals
	  • *component instances*
	  • instances of previously declared entity/architecture pairs
	  • *port maps* in component instances
	  • connect signals to component ports

7. test bench model
    - a model that uses the designed model
    - it applies test sequences to the inputs , monitors values on output signals and report error or warning messages.

Question (3) (35 Marks)

1- Write a VHDL code to implement the block diagram shown in Fig. 1 with its internal behavior as defined by the shown truth table. Write a test bench for it and draw the corresponding waveforms for your test cases. Assume signal types of BIT.
2- Use the structural way and write a VHDL code to construct 2 instances of Ckt_3 connected together with a common input clock.



in_1	in_2	in_3	ot_1	ot_2
0	x	x	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0

Fig. 1

Good Luck,
Dr. Ahmad El-Banna

Answer of Question (3)

Note: you can continue your answer in the back of the page.

1-

```
library ieee;
use ieee.std_logic_1164.all;
-----------------------------------------------------
entity Ckt_3 is
port(                   in1, in2, in3:    in bit;
                        ot1, ot2:          out bit
);
end Ckt_3 ;
-----------------------------------------------------
architecture behv of Ckt_3 is
begin
      process(in1, in2, in3)
   begin
      if (in1='0') then
                        ot1 <= '0';
                        ot2 <= '0';
      else
                        ot1 <= not in2;
                        ot2 <= not in3;
      end if;
   end process;
end behv;
```

---

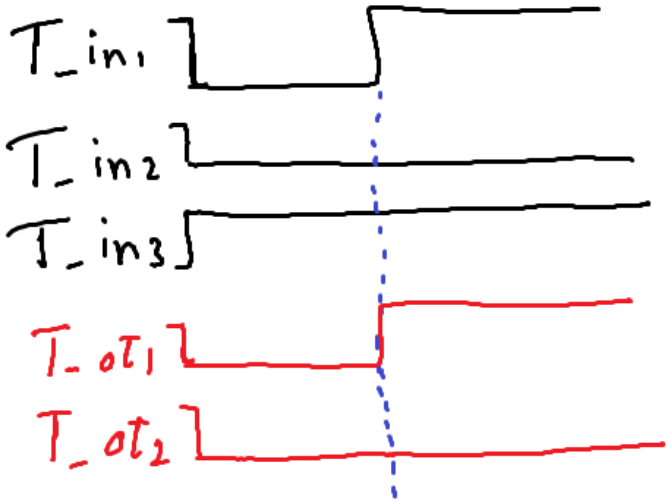
test bench:

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
entity Ckt_3 _TB is          -- empty entity
end Ckt_3 _TB;
```

```
architecture TB of  Ckt_3 _TB is

signal T_in1:bit:=’0’;
signal T_in2:bit:=’0’;
signal T_ in3:bit:=’0’;
signal T_ot1:bit;
signal T_ot1:bit;

component Ckt_3
port(                          in1, in2, in3:       in bit;
                               ot1, ot2:  out bit
);
end component;
begin
T_Ckt_3: Ckt_3 port map (T_in1, T_in2, T_in3, T_ot1, T_ot2);
process
variable err_cnt: integer :=0;
begin
T_in2<=’0’;
T_in3<=’1’;
-- case select eqaul ‘0’
                               wait for 10 ns;
                               T_in1 <= ‘0’;
                               wait for 1 ns;
                               assert (T_ot1=’0’) report "Error Case 0" severity error;
                            assert (T_ot2=’0’) report "Error Case 0" severity error;
                               if (T_ ot1/=’0’then
                                  err_cnt := err_cnt+1;
                               end if;
                            if (T_ ot2/=’0’then
                                  err_cnt := err_cnt+1;
                               end if;
-- case select equal ‘1’
                               wait for 10 ns;
                               T_in1 <= ‘1’;
                               wait for 1 ns;
                               assert (T_ot1=’1’) report "Error Case 0" severity error;
                            assert (T_ot2=’0’) report "Error Case 0" severity error;
                               if (T_ ot1/=’1’then
                                  err_cnt := err_cnt+1;
                               end if;
                            if (T_ ot2/=’0’then
                                  err_cnt := err_cnt+1;
                               end if;
-- summary of all the tests
                               if (err_cnt=0) then
                                  assert (false)
                                  report "Testbench of Mux completed sucessfully!"
                                  severity note;
                               else
                                  assert (true)
                                  report "Something wrong, try again!"
                                  severity error;
                               end if;
                               wait;
   end process;
end Ckt_3 _TB;
```



2-

```
architecture struct of Ckt_3 is
                        component Ckt_3
                                port ( in1,in2,in3, clk : in bit;  ot1,ot2 : out bit );
                        end component;
                        signal int_clk : bit;
begin
                        instance 1 : Ckt_3
                                port map ( in11,in12,in13, int_clk, ot11,ot12 );
                        instance 2 : Ckt_3
                                port map ( in21,in22,in23, int_clk, ot21,ot22 );
end struct;
```