Benha University
Faculty of Engineering at Shoubra
Electrical Engineering Department
Third Year (Communications)

Final Term Exam (Spring 2015)
Date: Monday (1/6/2015)
Subject: Electronic Circuits (B)
Duration: 4 hours

- **Significant equations sheet is attached.**
- **Answer all the following questions**

- **No. of questions : 5**
- **Total Mark: 90 Marks**

Model Answer

Question (1) (15 Marks)

Choose the correct answer:

1- The bandwidth of a dc amplifier having an upper critical frequency of 100 kHz is
(a) 100 kHz (b) unknown (c) infinity (d) 0 kHz

2- Bias current compensation
(a) reduces gain (b) reduces output error voltage (c) increases bandwidth (d) has no effect

3- Common-mode gain is
(a) very high (b) very low (c) always unity (d) unpredictable

4- Using output bounding in a comparator
(a) makes it faster (b) keeps the output positive (c) limits the output levels (d) stabilizes the output

5- For a step input, the output of an integrator is
(a) a pulse (b) a triangular waveform (c) a spike (d) a ramp

6- In an OTA, the transconductance is controlled by
(a) the dc supply voltage (b) the input signal voltage (c) the manufacturing process (d) a bias current

7- The damping factor of an active filter determines
(a) the voltage gain (b) the critical frequency (c) the response characteristic (d) the roll-off rate

8- A maximally flat frequency response is known as
(a) Chebyshev (b) Butterworth (c) Bessel (d) Colpitts

9- The operation of a relaxation oscillator is based on
(a) the charging and discharging of a capacitor (b) a highly selective resonant circuit
(c) a very stable supply voltage (d) low power consumption

10- All of the following are parts of a basic voltage regulator except
(a) control element (b) sampling circuit (c)voltage-follower (d) error detector (e)reference voltage

Question (2) (25 Marks)

1- What's the meaning of:

a. *Common-mode rejection* in a differential amplifier

A property means to provide attenuation of the unwanted common input while providing an amplified output of the difference signal applied to the inputs.

b. *Input offset voltage* in an op-amp.

It is the differential dc voltage required between the inputs to force the output to zero volts, Its primary cause is a slight mismatch of the base-emitter voltages of the differential amplifier input stage of an op-amp.

c. *Slew rate* in an op-amp.

It's the maximum rate of change of the output voltage in response to a step input voltage is the slew rate of an op-amp.

d. *Sallen-Key* Filter.

A second order circuit. It is used to provide very high Q factor and passband gain without the use of inductors. It is also known as a VCVS (voltage-controlled voltage source) filter.

e. *Line regulation.*

It's the percentage change in the output voltage for a given change in the input voltage.

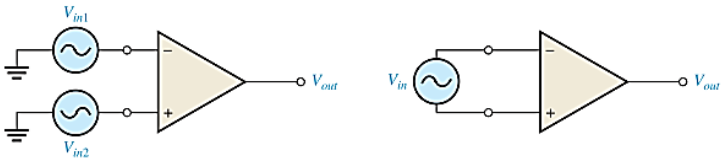
f. *Capture range* in PLL.

The capture range of a PLL is the frequency range centered about the VCO free-running frequency f_o over which the loop can acquire lock with the input signal.

2- What's the difference between differential mode and common mode of an op-amp?

Differential mode: two different signals on the input, A_d is very large.

Common mode: one common input to both inputs, A_c is very small



3- Compare between bjt transistor and op-amp amplifier circuits.

bjt transistor circuits

small signal amplifiers, dc signals can't be amplified, complex in determining the gain (depend on dc analysis), many discrete components are required i.e. design is somehow difficult, …etc.

op-amp amplifier circuits

dc amplifiers, easy to determine the gain by the external resistors (usually 2 resistors), easy design depending on IC circuit, provide high input impedance and low output impedance, can be used in many interface circuits, ..etc

4- What are the advantages of Active Filters?

Filters that use op-amps as the active element provide several advantages over passive filters (R, L, and C elements only).

- The op-amp provides gain, so the signal is not attenuated as it passes through the filter.
- The high input impedance of the op-amp prevents excessive loading of the driving source.
- The low output impedance of the op-amp prevents the filter from being affected by the load that it is driving.
- Active filters are also easy to adjust over a wide frequency range without altering the desired response.

5- What's the difference between linear regulators and switching regulators?

- The two types of linear regulators, series and shunt, have control elements (transistors) that are conducting all the time, with the amount of conduction varied as demanded by changes in the output voltage or current.
- The switching regulator is different because the control element operates as a switch.
- A much greater efficiency can be realized with a switching type of voltage regulator than with the linear types because the transistor switches on and off and dissipates power only when it is on.
- Switching regulators efficiencies can be greater than 90%.
- Three basic configurations of switching regulators are step-down, step-up, and inverting.

Question (3) (20 Marks)

1- Determine the output voltage waveform in Fig.1 .

Voltage across D_1 & D_2 = 4.7 + 0.7 = 5.4 V

$V_{R_2} = V_{out} - (V_{out} \pm 5.4\,V) = \pm 5.4\,V$

$I_{R_2} = \frac{V_{R_2}}{R_2} = \frac{\pm 5.4\,V}{47\,k\Omega} = \pm 0.11\,mA$

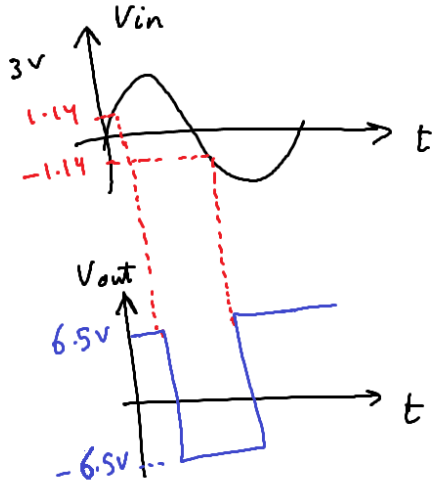
$I_{R_3} \simeq I_{R_2} = \pm 0.11\,mA$

$V_{R_3} = R_3 I_{R_3} = \pm 1.1\,V$

$V_{out} = V_{R_2} + V_{R_3} = \pm 6.5\,V$

$V_{UTP} = \left(\frac{R_3}{R_2+R_3}\right)(+V_{out}) = +1.14\,V$

$V_{LTP} = \left(\frac{R_3}{R_2+R_3}\right)(-V_{out}) = -1.14\,V$



2- For the circuit shown in Fig. 2:

a. Determine the critical frequency.

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} = \frac{1}{2\pi\sqrt{R_5R_6C_3C_4}} = \frac{1}{2\pi\sqrt{(4.7\,k\Omega)(6.8\,k\Omega)(0.22\,\mu F)(0.1\,\mu F)}} = \mathbf{190\ Hz}$$

b. Determine the order and the type of this filter.

4th order & LPF

c. Make the necessary changes to make this circuit works as a BPF with B.W. of 2 kHz around the center frequency calculated in (a), then determine:

i. The Damping factor.

ii. The Quality factor of this filter.

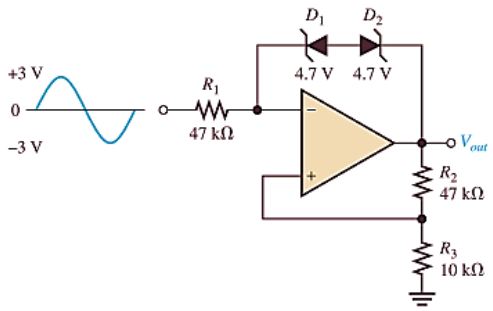


Fig. 1

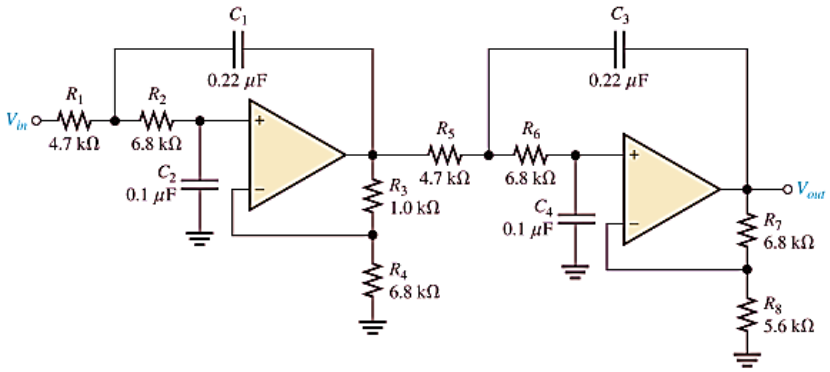


Fig. 2

To work as BPF 2nd order:

Replace the capacitors C_1,C_2 with the resistors R_1,R_2 *or* replace the capacitors C_3,C_4 with the resistors R_5,R_6

To work as BPF 4th order:

Add a 4th order HPF before or after this circuit, HPF is constructed by replacing the position of the resistors and capacitors.

The cutoff frequencies of the LPF & HPF will be 190+1K Hz , 190-1K Hz respectively (assume 190-1k equals 0Hz), then determine a suitable C value assuming the R values are the same and equal 1K.

i. Damping Factor

1st stage:

$$DF = 2 - \frac{R_3}{R_4} = 2 - \frac{1.0\,\text{k}\Omega}{6.8\,\text{k}\Omega} = 1.85$$

2nd stage:

$$DF = 2 - \frac{R_7}{R_8} = 2 - \frac{6.8\,\text{k}\Omega}{5.6\,\text{k}\Omega} = 0.786$$

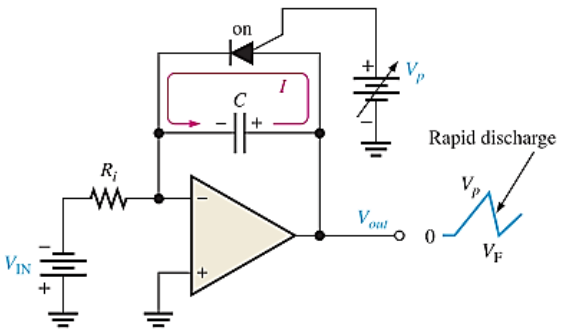
ii. Quality Factor

$$Q = \frac{f_0}{BW}$$

Q= 190/2k=0.095 (bad Q)

Question (4) (15 Marks)

1- Design a 1 kHz : 10 MHz sawtooth VCO circuit.



Using the shown circuit with frequency:

$$f = \frac{|V_{IN}|}{R_i C}\left(\frac{1}{V_p - V_F}\right)$$

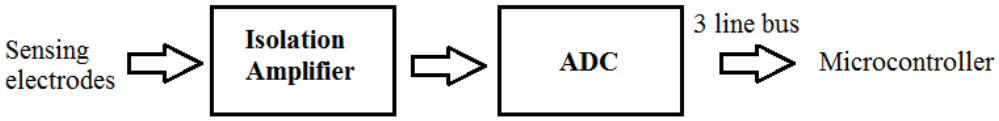
Select Ri=10k, C = 1 uF

Assume Vf=0.7 & V_p = 9V battery

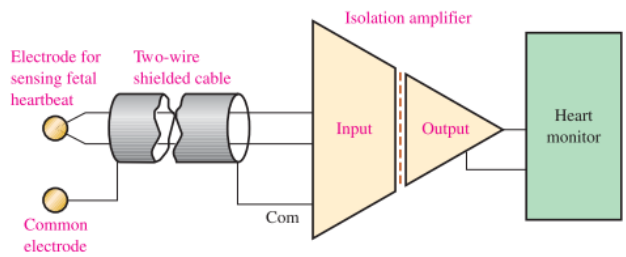
Choose values for V_{IN} to cover the required range

1 kHz : 10 MHz

2- Design an interface circuit that transmits a heart beats signal with peak value of 4.9 mV from the sensing electrodes to a microcontroller unit through a 3 line bus. (*Hint: you should build two blocks in this circuit*)

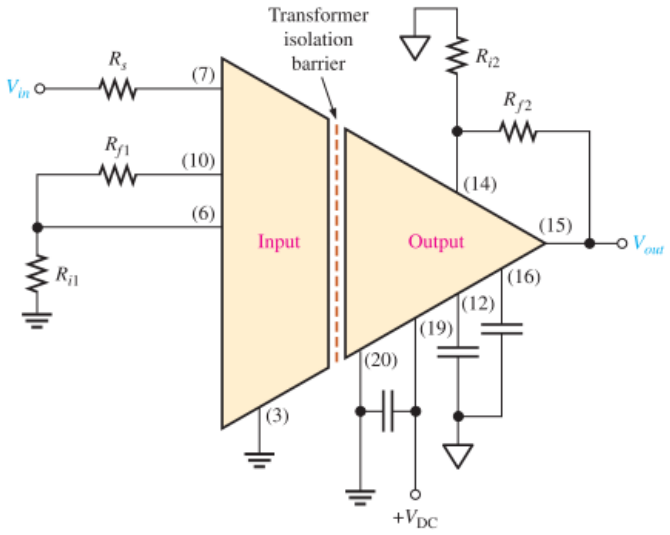


Isolation amplifier



ADC

Using Vref of 5v and R of 10 K in the below figure

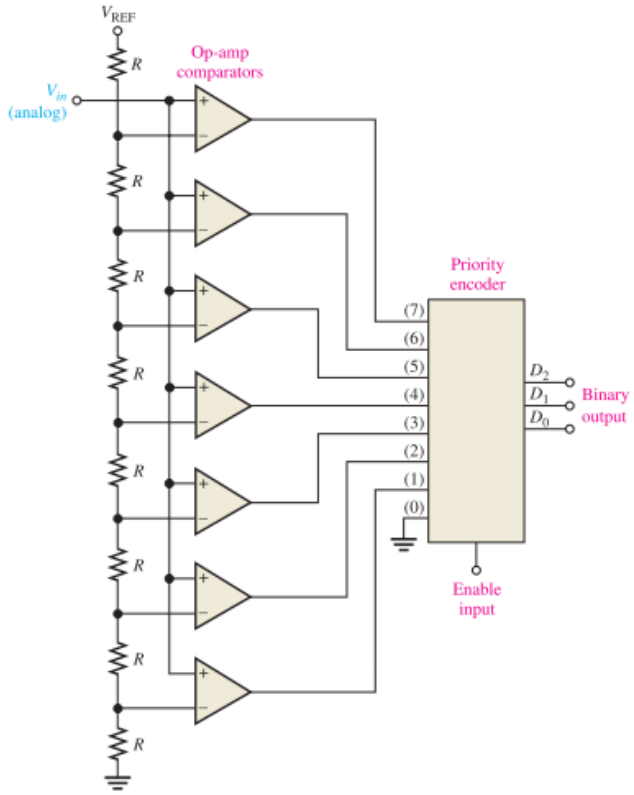


Using the equations

$$A_{v1} = \frac{R_{f1}}{R_{i1}} + 1$$

$$A_{v2} = \frac{R_{f2}}{R_{i2}} + 1$$

Select the resistor values R_f, R_i for a suitable overall (Av1*Av2) gain of 10 e.g. $R_{f1}= R_{i1}= R_{i2}=1k$; $R_{f2}=4k$
Use suitable supply of 12 v, Rs = 10 k, and capacitors values of 0.47 uF.

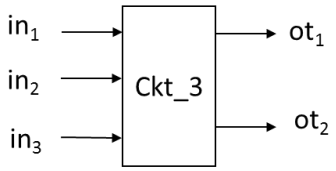


Question (5) (15 Marks)

1- Give two applications of the Hardware Description Language (HDL).
   - Model and document digital systems
     - Different levels of abstraction e.g. behavioral, structural, etc.
   - Verify design
   - Synthesize circuits
     - Convert from higher abstraction levels to lower abstraction levels

2- What is a test bench model?
   - a model that uses the designed model
   - it applies test sequences to the inputs , monitors values on output signals and report error or warning messages.

3- Write a VHDL code to implement the block shown in Fig. 3 with its internal behavior as defined by the shown truth table. Assume signal types of BIT.



in_1	in_2	in_3	ot_1	ot_2
0	x	x	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0

Fig. 3

```
library ieee;
use ieee.std_logic_1164.all;
--------------------------------------------------
entity Ckt_3 is
port(                   in1, in2, in3:    in bit;
                        ot1, ot2:          out bit
);
end Ckt_3;
--------------------------------------------------
architecture behv of Ckt_3 is
begin
      process(in1, in2, in3)
   begin
      if (in1='0') then
                        ot1 <= '0';
                        ot2 <= '0';
      else
                        ot1 <= not in2;
                        ot2 <= not in3;
      end if;
   end process;
end behv;
```

Good Luck,
Dr. Ahmad El-Banna