Benha University
Faculty of Engineering at Shoubra
Electrical Engineering Department
Third Year (Communications)

Final Term Exam (Spring 2016)
Date: Saturday (28/5/2016)
Subject: Electronic Circuits (B)
Duration: 4 hours

- **Significant equations sheet is attached.**
- **Answer all the following questions**

- **No. of questions : 5**
- **Total Mark: 90 Marks**

Model Answer

Question (1) (15 Marks)

Choose the correct answer:

1- With zero volts on both inputs, an op-amp ideally should have an output equal to
(a) the positive supply voltage (b) the negative supply voltage (c) zero (d) the CMRR

2- The frequency at which the open-loop gain is equal to 1 is called
(a) the upper critical frequency (b) the cutoff frequency (c) the notch frequency (d) the unity-gain frequency

3- All isolation amplifiers use transformer coupling.
(a) True (b) False

4- Instrumentation amplifiers are used primarily in
(a) high-noise environments (b) medical equipment (c) test instruments (d) filter circuits

5- An OTA is basically a
(a) voltage-to-current amplifier (b) current-to-voltage amplifier (c) current-to-current amplifier
(d) voltage-to-voltage amplifier

6- The number of poles in a filter affect the
(a) voltage gain (b) bandwidth (c) center frequency (d) roll-off rate

7- Sallen-Key low-pass filters are
(a) single-pole filters (b) second-order filters (c) Butterworth filters (d) band-pass filters

8- The main purpose of current limiting in a regulator is
(a) protection of the regulator from excessive current (b) protection of the load from excessive current
(c) to keep the power supply transformer from burning up (d) to maintain a constant output voltage

9- Linear and switching are two main categories of voltage regulators.
(a) True (b) False

10- The lock range in the PLL is….. the capture range.
(a) Equals to (b) greater than (c) smaller than

Question (2) (25 Marks)

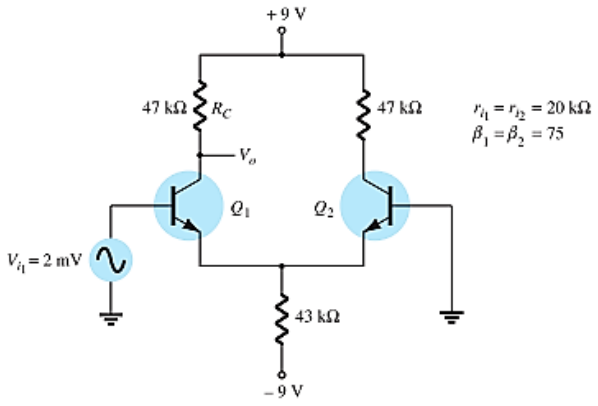


Fig. 1

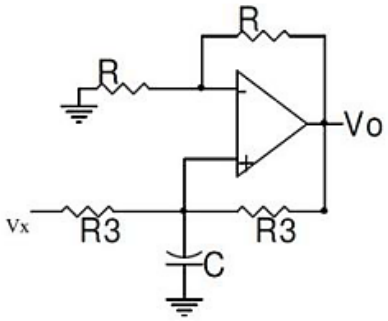


Fig. 2

1- For the circuit shown in **Fig.1**,
   a. Calculate the following:
      i. The single ended output voltage V_o for the circuit.
      ii. The common-mode gain for the amplifier circuit.
   b. Constant current source is usually used with this circuit, draw such circuit and state why?

Answer:

a.

Solution: The dc bias calculations provide

$$I_E = \frac{V_{EE} - 0.7\text{ V}}{R_E} = \frac{9\text{ V} - 0.7\text{ V}}{43\text{ k}\Omega} = 193\ \mu\text{A}$$

The collector dc current is then

$$I_C = \frac{I_E}{2} = 96.5\ \mu\text{A}$$

so that $V_C = V_{CC} - I_C R_C = 9\text{ V} - (96.5\ \mu\text{A})(47\text{ k}\Omega) = 4.5\text{ V}$

The value of r_e is then

$$r_e = \frac{26}{0.0965} \cong 269\ \Omega$$

The ac voltage gain magnitude can be calculated using Eq. (10.31):

$$A_v = \frac{R_C}{2r_e} = \frac{(47\text{ k}\Omega)}{2(269\ \Omega)} = 87.4$$

providing an output ac voltage of magnitude

$$V_o = A_v V_i = (87.4)(2\text{ mV}) = 174.8\text{ mV} = \mathbf{0.175\text{ V}}$$

$$A_c = \frac{V_o}{V_i} = \frac{\beta R_C}{r_i + 2(\beta + 1)R_E} = \frac{75(47\text{ k}\Omega)}{20\text{ k}\Omega + 2(76)(43\text{ k}\Omega)} = \mathbf{0.54}$$

b.

- A good differential amplifier has a very large difference gain A_d, which is much larger than the common-mode gain A_c.
- The common-mode rejection ability of the circuit can be considerably improved by making the common-mode gain as small as possible (ideally, 0)
- The larger R_E, the smaller is A_c.
- One popular method for increasing the ac value of R_E is using a constant-current source circuit.

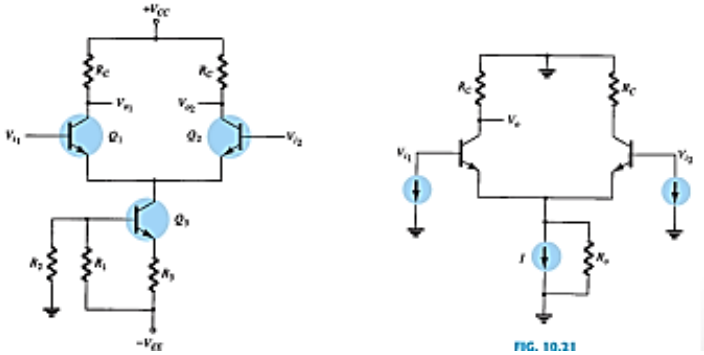
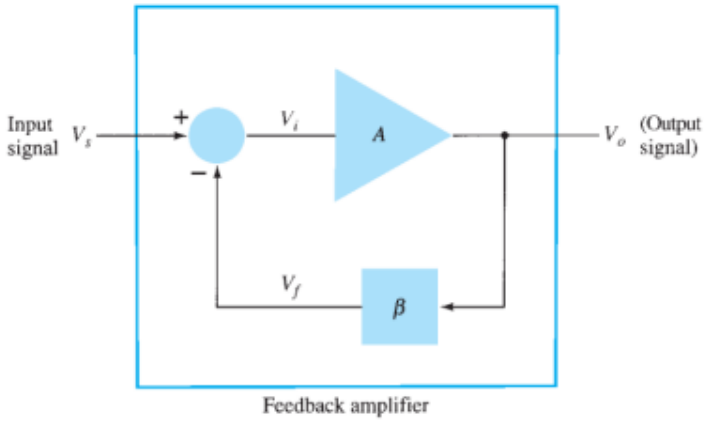


FIG. 10.21

2- Sketch the block diagram of the feedback amplifier and list the advantages of negative feedback.

Answer:



Feedback amplifier

The advantages are:

i. Higher input impedance.
ii. Better stabilized voltage gain.
iii. Improved frequency response.
iv. Lower output impedance.

3- Prove that the closed loop gain in the non-inverting Op-amp circuit is

$$A_{CL} = 1 + \frac{R_f}{R_i}.$$

Answer:

$$V_f = \left(\frac{R_i}{R_i + R_f}\right)V_{out}$$

$$V_{out} = A_{ol}(V_{in} - V_f)$$

$$B = \frac{R_i}{R_i + R_f}$$

$$V_{out} = A_{ol}(V_{in} - BV_{out})$$

$$V_{out} = A_{ol}V_{in} - A_{ol}BV_{out}$$

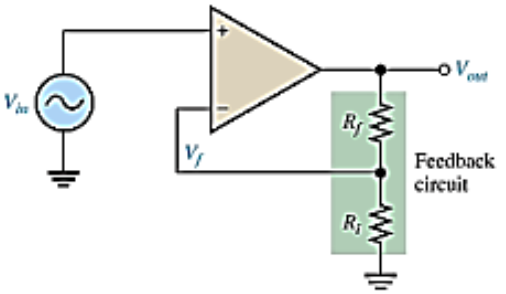
$$V_{out} + A_{ol}BV_{out} = A_{ol}V_{in}$$

$$V_{out}(1 + A_{ol}B) = A_{ol}V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{A_{ol}}{1 + A_{ol}B}$$

$$\frac{V_{out}}{V_{in}} \cong \frac{A_{ol}}{A_{ol}B} = \frac{1}{B}$$

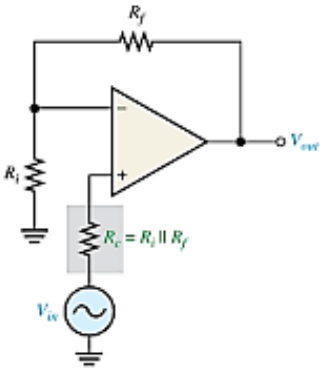
$$A_{cl(NI)} = \frac{V_{out}}{V_{in}} \cong \frac{1}{B} = \frac{R_i + R_f}{R_i}$$



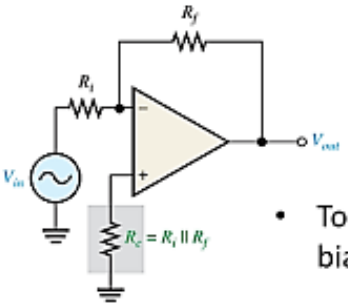
$$A_{cl(NI)} = 1 + \frac{R_f}{R_i}$$

4- Show how you can compensate for bias current and input offset voltage in Op-amp circuits.

Answer:



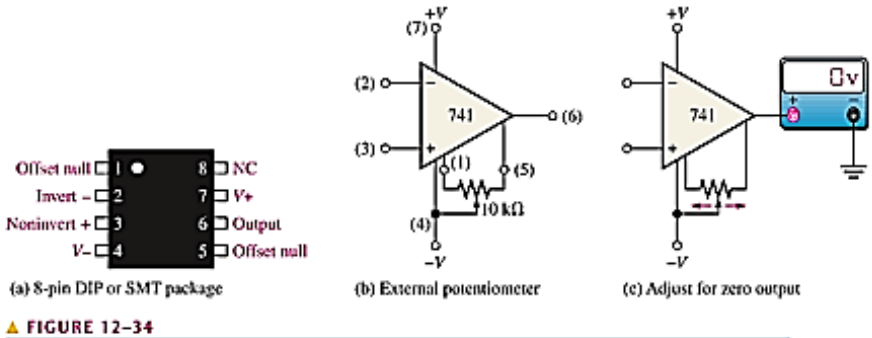
(a) Noninverting amplifier



(b) Inverting amplifier

- To compensate for the effect of bias , a resistor Rc is added.
- Use of a BIFET Op-Amp to Eliminate the Need for Bias Current Compensation

Input Offset Voltage Compensation



(a) 8-pin DIP or SMT package (b) External potentiometer (c) Adjust for zero output

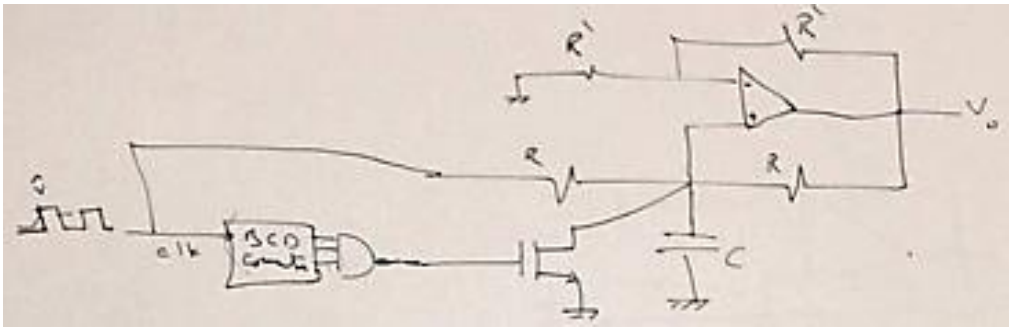
▲ FIGURE 12–34

Input offset voltage compensation for a 741 op-amp.

5- For the circuit shown in **Fig.2**, show how can you use it to generate a staircase waveform. What's the step voltage assuming R=2KΩ, R3= 6KΩ, C= 10 uF.

Answer:

Use the following circuit to generate a staircase:



The step voltage = $(2/RC)*V_{in}\ t = (2/6K*10u)*V_{in}\ t = 33.3\ V_{in}\ t$

Question (3) (20 Marks)

1- Give three different classifications of filters.

Answer:

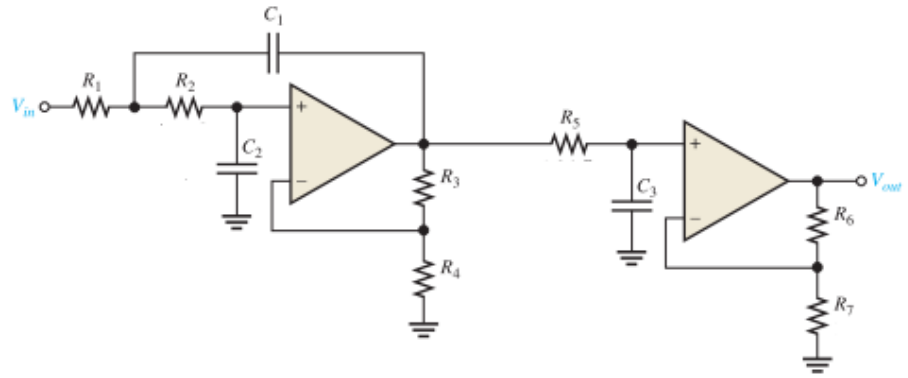
Different classifications of filters include:

1) LPF, HPF, BPF and BSF
2) 1st order (1-pole), 2nd order (2-pole), 3rd order (3-pole),…, nth order (n-pole)
3) Butterworth, Chebychev and Bessel.
4) Active & Passive

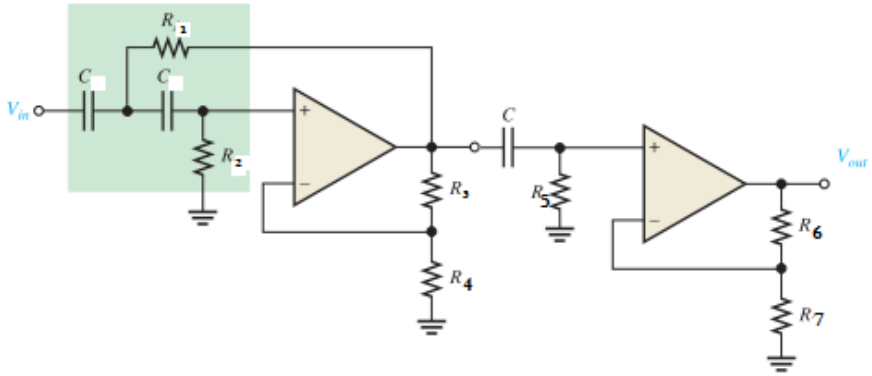
2- Design a 3rd order Butterworth BPF with center frequency of 98 KHz and a quality factor of 15 and a gain of 20dB.

Answer:

The band pass filter consists of cascading LPF with HPF.
For a 3rd order BPF, we need 3rd order LPF and 3rd order HPF.
The LPF is:

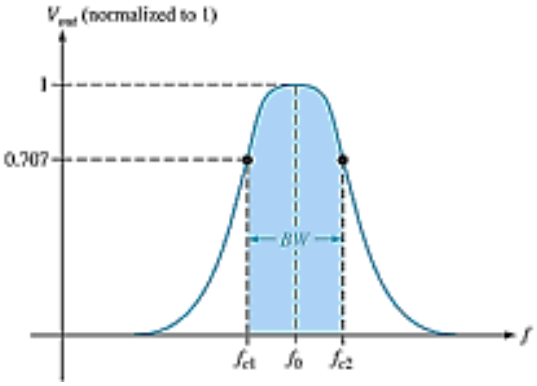


The HPF is:



For Butterworth filter, from attached table
R3/R4=1& R6/R7=1
Use equal resistors R6=R7=R3=R4=1K ohm

The BPF response is as shown



fo=98K,Q=15 therefore → BW=fo/Q=98K/15= 6.5K

The LPF cutoff frequency = fc2=fo + (BW/2)= 98+3.25=101.25 KHz
Using C1=C2=C3=C=1 uF , the resistors in the LPF can be calculated from f=1/2*pi*R*C

The HPF cutoff frequency = fc1=fo - (BW/2)= 98-3.25=95.25 KHz
Using C1=C2=C3=C=1 uF , the resistors in the HPF can be calculated from f=1/2*pi*R*C

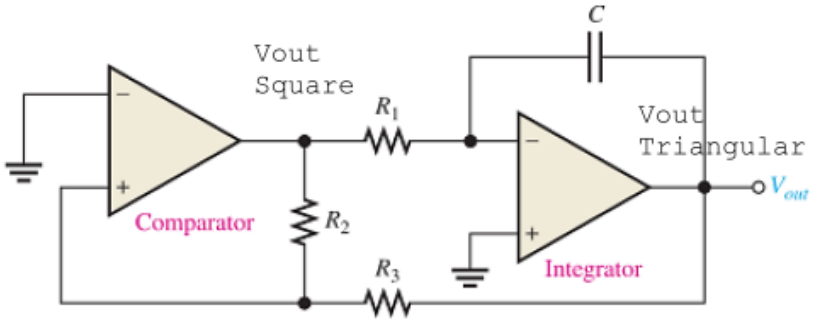
For gain of 30dB which equals 31.6 in ratio, we can add a non inverting amplifier with resistors as

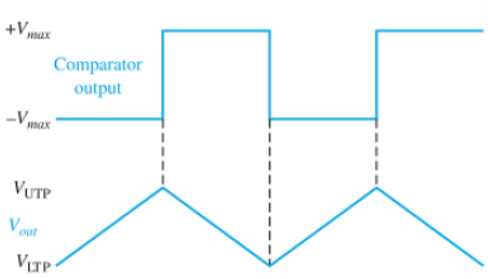
Rf/Ri= 32.6 , using Ri=1K so Rf= 32.6K

3- Construct a function generator circuit that provides square and triangular waveforms with 35 KHz frequency. Determine the amplitude of each waveform.

Answer:

Many designs can be used using op-amp circuits or 555 timers, one design is using two op-amps





The amplitude and frequency can be calculate using

$$f_r = \frac{1}{4R_1C}\left(\frac{R_2}{R_3}\right)$$

Then using the frequency =35K and for example C= 10 uF, R2=R3=1K we can choose suitable values for the other resistor R1 from the above equation.

The amplitude for the square equals the supply voltage for example 9V and the amplitude eof the triangle is calculated from

$$V_{\text{UTP}} = +V_{max}\left(\frac{R_3}{R_2}\right)$$

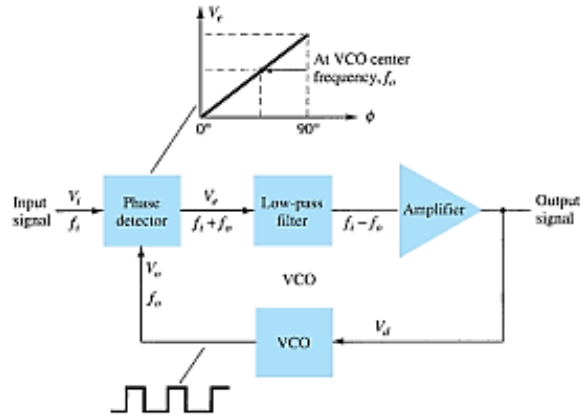
$$V_{\text{LTP}} = -V_{max}\left(\frac{R_3}{R_2}\right)$$

Choosing R3=R2 sets the triangle amplitude equals the supply voltage for example 9V.

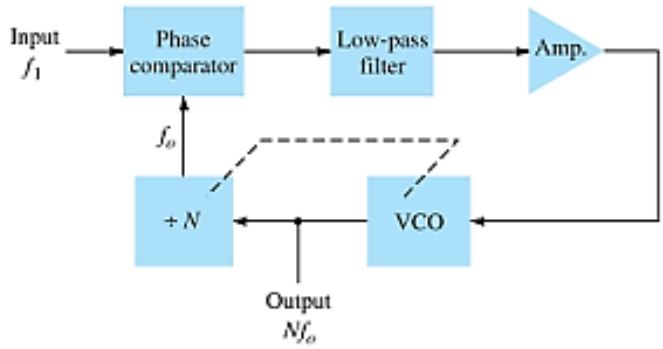
4- Sketch the internal construction of the PLL and show how you can use it as a frequency synthesis.

Answer:

The internal construction of the PLL is



To use it as frequency synthesis add a divide by N network as shown

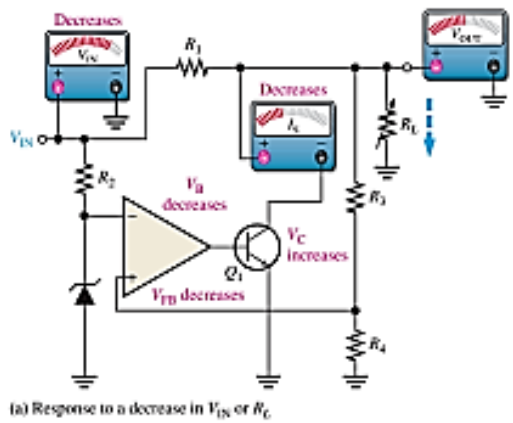


Question (4) (20 Marks)

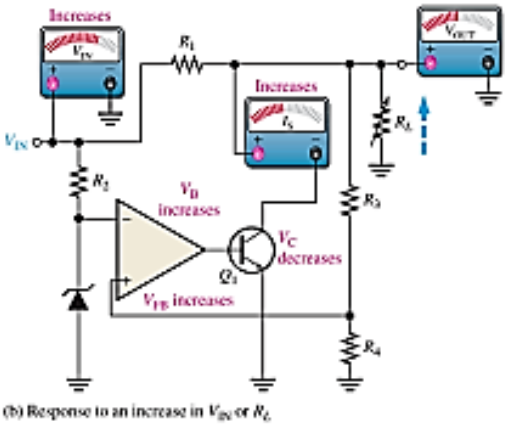
1- Discuss the regulation action in the shunt voltage regulator.

Answer:

- Sequence of responses when V_{OUT} tries to decrease as a result of a decrease in R_L or V_{IN} (opposite responses for an attempted increase)



(a) Response to a decrease in V_{IN} or R_L



(b) Response to an increase in V_{IN} or R_L

2- Design a circuit to produce:

$$v_o = \frac{v_{i1} + v_{i2} + v_{i3}}{3} - 0.025 \ln 0.5 v_{i4} + 10^3 \int v_{i5}\, dt$$

Answer:

Many designs are available

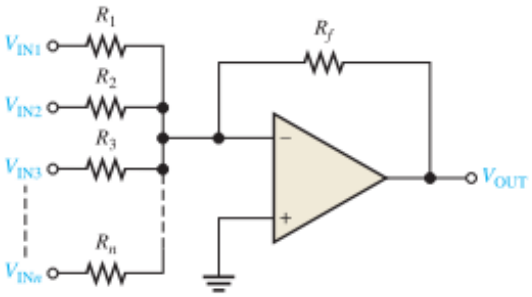
We use a summer amplifier to add the terms together as follows,

The first term is average amplifier with three inputs and the second is logarithmic amplifier and the third is non inverting integrator or an inverting integrator followed by an inverting amplifier

We select suitable components R and C dpending on each term value.

The individual circuits are

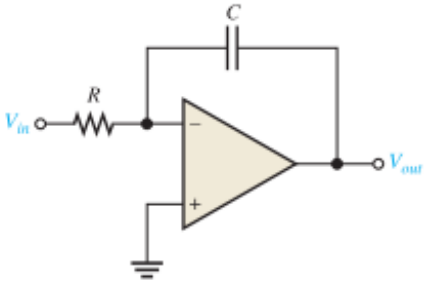
Summer→



$$V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3} + \cdots + V_{INn})$$

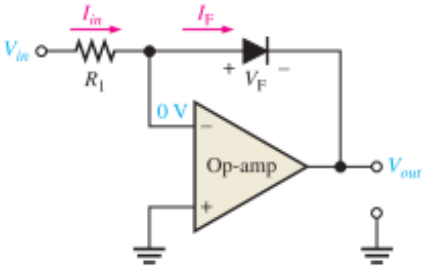
And averaging amplifier is the same but with $\frac{R_f}{R} = \frac{1}{n}$

Integrator→



$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}$$

Log-Amp→



$$V_{out} \cong -(0.025\ \text{V}) \ln\left(\frac{V_{in}}{I_R R_1}\right)$$

3- Using the characteristics of a simple PTC (Positive Temperature Coefficient) Temperature Sensor (T.S.) shown in **Fig.3**, design the interface circuits shown in **Fig.4**:

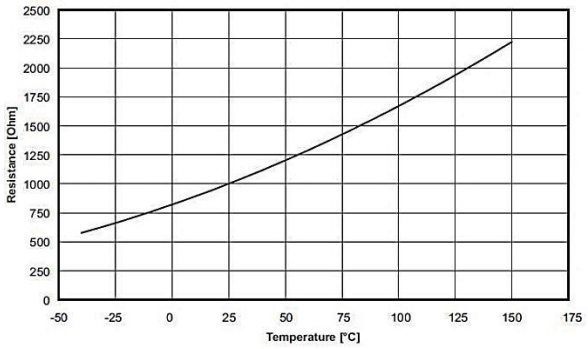


Fig.3

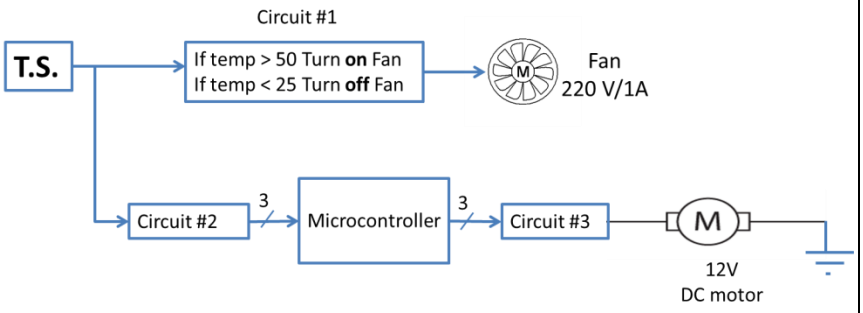


Fig.4

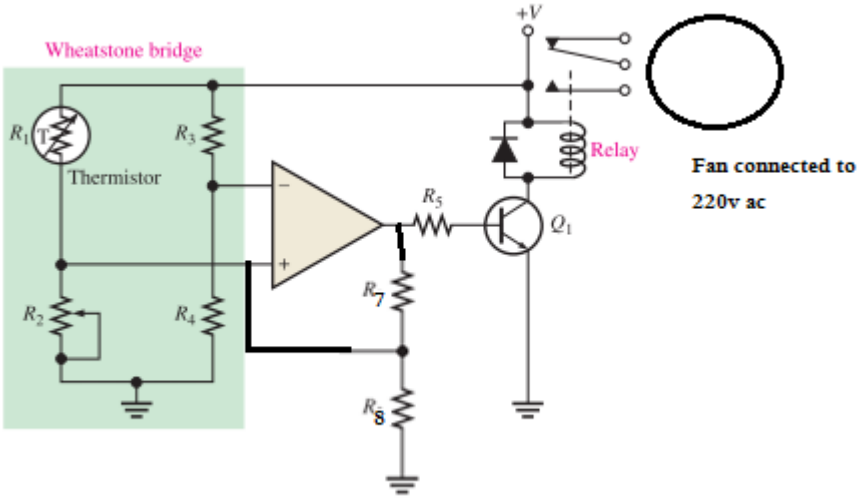
Answer:

From Fig.3 , at T=25,50 → the sensor resistance is R=1k, 1.2K respectively.

Many designs are available but the main idea is as follows

Circuit#1 is shmitt trigger, a comparator with hystresis

Put the sensor (thermistor) with Resistor as voltage divider branch then take the common as the input to this sircuit as shown

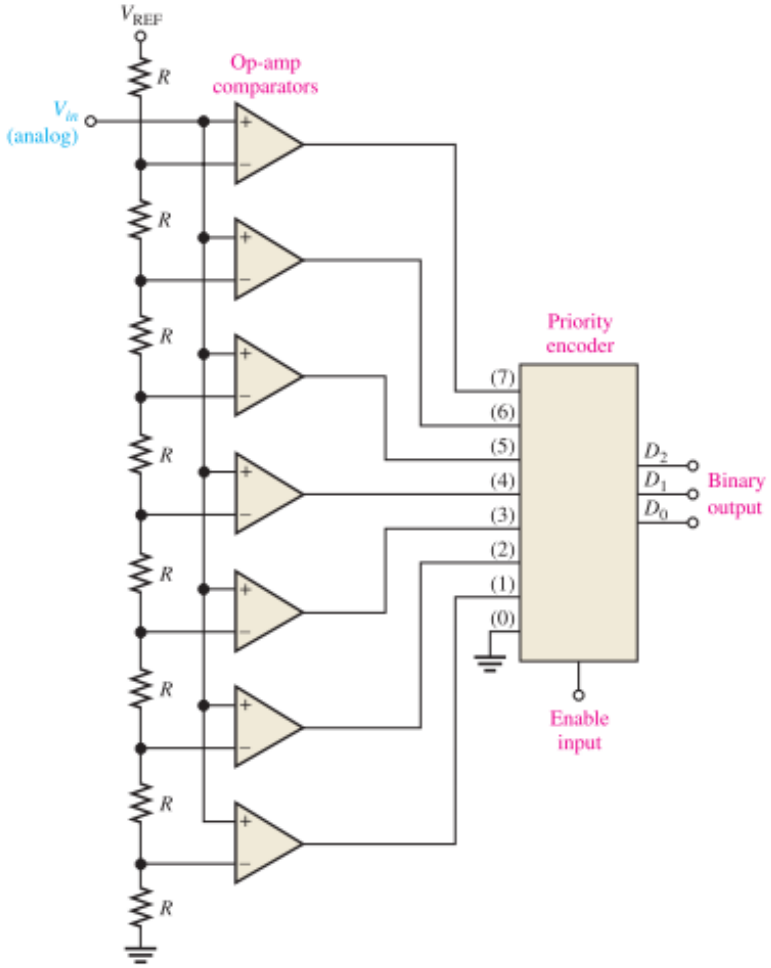


Use V=12V, R2 pot =10K, R3=R4=R5=1K choose suitable R7,R8 depending on the hystresis as

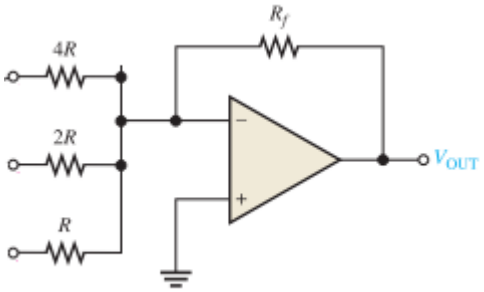
$$V_{LTP} = \frac{R_8}{R_7 + R_8}(-V) \quad \& \quad V_{UTP} = \frac{R_8}{R_7 + R_8}(V)$$

Circuit#2 is 3-bit ADC

Use Vref=12V and R=1K



Circuit # 3 is 3-bit DAC
Use R=Rf=1K,Vref >12V.



Question (5) (10 Marks)

1- List the three ways used to implement a VHDL code.

Answer:
The three ways are:

a) Data flow
b) Combinational
c) Structure way

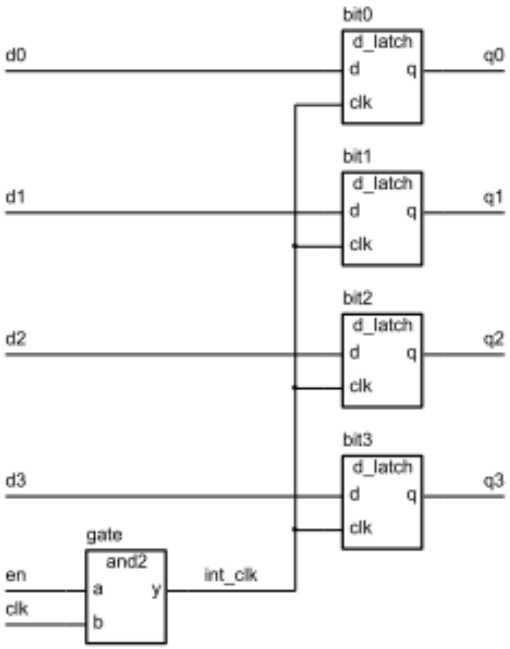
2- Write a VHDL code to implement only one of the following:

(a) 4-bit register.

(b) Dual 4-bit ALU connected to a MUX.

Answer:

The student can choose any system of the above. For example the 4-bit register and implement it as follows



- First **declare D-latch** and **and-gate** entities and architectures

```
entity d_latch is
    port ( d, clk : in bit;  q : out bit );
end entity d_latch;

architecture basic of d_latch is
begin
    process (clk, d)
    begin
        if clk = '1' then
            q <= d after 2 ns;
        end if;
    end process;
end basic;
```

```
entity and2 is
    port ( a, b : in bit;  y : out bit );
end entity and2;

architecture basic of and2 is
begin
    process (a, b)
    begin
        y <= a and b after 2 ns;
    end process ;
end basic;
```

- **Declare** corresponding **components** in register architecture body

```
architecture struct of reg4 is
    component d_latch
        port ( d, clk : in bit;  q : out bit );
    end component;
    component and2
        port ( a, b : in bit;  y : out bit );
    end component;
    signal int_clk : bit;
...
```

```
...
begin
    bit0 : d_latch
        port map ( d0, int_clk, q0 );
    bit1 : d_latch
        port map ( d1, int_clk, q1 );
    bit2 : d_latch
        port map ( d2, int_clk, q2 );
    bit3 : d_latch
        port map ( d3, int_clk, q3 );
    gate : and2
        port map ( en, clk, int_clk );
end struct;
```

Good Luck,

Dr. Ahmad El-Banna

Formula equations

***Operational Amplifiers:** $I_E = \{v_E - (-v_{EE})\}/R_E$. , $I_c = \frac{I_E}{2}$. , $V_c = V_{cc} - \left(\frac{I_E}{2}\right)R_c$. , $I_b = \frac{V_i}{2\beta r_e}$. $I_c = \frac{V_i}{2r_e}$, single ended: $A_v = \frac{R_c}{2r_e}$, double ended: $A_d = \frac{V_o}{V_d} = \frac{R_c}{r_e}$, common mode: $A_c = \frac{\beta R_c}{[r_i + 2(\beta+1)R_E]}$. $V_d = V_{i_1} - V_{i_2}$. $\mathbf{CMRR} = \frac{A_{ol}}{A_{cm}}$, $\mathbf{CMRR} = \mathbf{20\log}\left(\frac{A_{ol}}{A_{cm}}\right)$, $I_{\mathbf{BIAS}} = \frac{I_1 + I_2}{2}$, $I_{\mathbf{OS}} = |I_1 - I_2|$, $V_{\mathbf{OS}} = I_{\mathbf{OS}}R_{in}$, $V_{\mathbf{OUT(error)}} = A_v I_{\mathbf{OS}}R_{in}$, $\mathbf{Slew\ rate} = \frac{\Delta V_{out}}{\Delta t}$ $\boxed{A_f = \frac{A}{1 + \beta A}}$ $\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right|$ ↣Non-Inverting Amplifiers : $V_f = \left(\frac{R_i}{R_i + R_f}\right)V_{out}$, $V_{out} = A_{ol}(V_{in} - BV_{out})$, $A_{cl(\mathrm{NI})} = 1 + \frac{R_f}{R_i}$, $Z_{out(\mathrm{NI})} = \frac{Z_{out}}{1 + A_{ol}B}$, $Z_{in(\mathrm{NI})} = (1 + A_{ol}B)Z_{in}$ .Inverting Amplifiers : $A_{cl(\mathrm{I})} = -\frac{R_f}{R_i}$, $Z_{in(\mathrm{I})} \cong R_i$, $A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + f^2/f_c^2}}$ $Z_{out(\mathrm{I})} = \frac{Z_{out}}{1 + A_{ol}B}$. $Z_{in(\mathrm{VF})} = (1 + A_{ol})Z_{in}$, $Z_{out(\mathrm{VF})} = \frac{Z_{out}}{1 + A_{ol}}$, $BW = f_{cu}$, , $\theta = -\tan^{-1}\left(\frac{f}{f_c}\right)$, $\theta_{tot} = -\tan^{-1}\left(\frac{f}{f_{c1}}\right) - \tan^{-1}\left(\frac{f}{f_{c2}}\right) - \tan^{-1}\left(\frac{f}{f_{c3}}\right)$ $f_{c(cl)} = f_{c(ol)}(1 + BA_{ol(mid)})$, $BW_{cl} = BW_{ol}(1 + BA_{ol(mid)})$, $f_T = A_{cl}f_{c(cl)}$ ***Basic Op-Amp Circuits** $V_{\mathrm{UTP}} = \frac{R_2}{R_1 + R_2}(+V_{out(max)})$, $V_{\mathrm{LTP}} = \frac{R_2}{R_1 + R_2}(-V_{out(max)})$, $V_{\mathbf{HYS}} = V_{\mathbf{UTP}} - V_{\mathbf{LTP}}$ Summing Amplifier: $V_{\mathbf{OUT}} = -\frac{R_f}{R}(V_{\mathrm{IN1}} + V_{\mathrm{IN2}} + \cdots + V_{\mathrm{IN}n})$.↣averaging: $\frac{R_f}{R} = \frac{1}{n}$ ↣scaling: $V_{\mathbf{OUT}} = -\left(\frac{R_f}{R_1}V_{\mathrm{IN1}} + \frac{R_f}{R_2}V_{\mathrm{IN2}} + \cdots + \frac{R_f}{R_n}V_{\mathrm{IN}n}\right)$ ↣DAC: I_0=+V/8R,, I_1=+V/4R,, I_2=+V/2R,, I_3=+V/R,,, $V_{out(D0,1,2,3)}$=-R_f $I_{0,1,2,3}$↣ Integrator Amplifier: $\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}$.↣ Differentiator Amplifier: $V_{out} = -\left(\frac{V_C}{t}\right)R_f C$.↣ Non-Inverting Integrator Amplifier: $v_o(t) = (2/CR_3) * \int_0^t v_x\ dt$ ***Special-purpose Op-amp Circuits:**

↣instrumentation amplifier : $A_{cl} = 1 + \frac{2R}{R_G}$, $R_G = \frac{2R}{A_{cl} - 1}$ ↣isolation amplifier: $A_{v1} = \frac{R_{f1}}{R_{i1}} + 1$, $A_{v2} = \frac{R_{f2}}{R_{i2}} + 1$, $A_{v(tot)} = A_{v1}A_{v2}$ ↣OTA: gm=Iout/v , $g_m = KI_{\mathbf{BIAS}}$, $A_v = g_m R_L$, $I_{\mathrm{BIAS}} = \frac{+V_{\mathrm{BIAS}} - (-V) - 1.4\,\mathrm{V}}{R_{\mathrm{BIAS}}}$

↣Log Amplifiers: $I_F \cong I_R e^{qV_F/kT}$ $V_F = \left(\frac{kT}{q}\right)\ln\left(\frac{I_F}{I_R}\right)$ $V_{out} \cong -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_R R_1}\right)$,

$V_{out} = -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_{EBO}R_1}\right)$ ↣Anti-Log Amplifiers: $V_{out} = -R_f I_{EBO}\text{antilog}\left(\frac{V_{in}}{25\text{ mV}}\right)$

↣Constant-Current Source: $I_L = \frac{V_{IN}}{R_i}$.↣Current-to-Voltage Converter: $V_{out} = I_i R_f$

↣ Voltage -to- Current Converter: $I_L = \frac{V_{in}}{R_1}$ ***Active Filters:**

↣LPF: $BW = f_c$ $f_c = \frac{1}{2\pi RC}$ ↣BPF: $BW = f_{c2} - f_{c1}$ $f_0 = \sqrt{f_{c1}f_{c2}}$

$Q = \frac{f_0}{BW}$ $Q = \frac{1}{DF}$ $DF = 2 - \frac{R_1}{R_2}$ ↣Single pole LPF: $f_c = \frac{1}{2\pi\sqrt{R_A R_B C_A C_B}}$

$A_{cl(NI)} = \frac{R_1}{R_2} + 1$ ↣Sallen-key LPF: ↣Cascade BPF: $f_{c1} = \frac{1}{2\pi\sqrt{R_{A1}R_{B1}C_{A1}C_{B1}}}$

$f_{c2} = \frac{1}{2\pi\sqrt{R_{A2}R_{B2}C_{A2}C_{B2}}}$ $f_0 = \sqrt{f_{c1}f_{c2}}$ ↣Multiple feedback: $f_0 = \frac{1}{2\pi C}\sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}}$

$R_2 = \frac{Q}{\pi f_0 C}$ $R_3 = \frac{Q}{2\pi f_0 C(2Q^2 - A_0)}$ $A_0 = \frac{R_2}{2R_1}$ $R_1 = \frac{Q}{2\pi f_0 C A_0}$ ↣State variable

filter: $Q = \frac{1}{3}\left(\frac{R_5}{R_6} + 1\right)$ ***Signals Generators:**↣Triangular: $V_{UTP} = +V_{max}\left(\frac{R_3}{R_2}\right)$ $V_{LTP} = -V_{max}\left(\frac{R_3}{R_2}\right)$

$f_r = \frac{1}{4R_1 C}\left(\frac{R_2}{R_3}\right)$ ↣Sawtooth: $T = \frac{V_p - V_F}{|V_{IN}|/R_i C}$ f=1/T ,, $f = \frac{|V_{IN}|}{R_i C}\left(\frac{1}{V_p - V_F}\right)$

↣555: $f_r = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$ $\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right)100\%$

Using D1:

$f_r \cong \frac{1.44}{(R_1 + R_2)C_{ext}}$

$\text{Duty cycle} \cong \left(\frac{R_1}{R_1 + R_2}\right)100\%$ T(high)=0.694(R1+R2)Cext ,, T(low)=0.694(R2)Cext ,,

T=Th+Tl=0.694(R1+2R2)Cext ***Voltage Regulator:**

$\text{Line regulation} = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right)100\%$ $\text{Line regulation} = \frac{(\Delta V_{OUT}/V_{OUT})100\%}{\Delta V_{IN}}$ $\text{Load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right)100\%$

$\text{Load regulation} = \left(\frac{R_{OUT}}{R_{FL}}\right)100\%$ Series: $V_{OUT} \cong \left(1 + \frac{R_2}{R_3}\right)V_{REF}$ $I_{L(max)} = \frac{0.7\text{ V}}{R_4}$

↣Shunt: $\Delta I_S = \frac{\Delta V_{IN}}{R_1}$ $I_{L(max)} = \frac{V_{IN}}{R_1}$ ***PLL :**↣ Frequency demodulator $f_o = \frac{0.3}{R_1 C_1}$

↣ lock range $f_L = \pm\frac{8f_o}{V}$ ↣ capture range $f_C = \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_2 C_2}}$

→ (Values for the Butterworth filter response)

ORDER	ROLL-OFF DB/DECADE	1ST STAGE			2ND STAGE			3RD STAGE		
		POLES	*DF*	R_1/R_2	POLES	*DF*	R_3/R_4	POLES	*DF*	R_5/R_6
1	−20	1	Optional							
2	−40	2	1.414	0.586						
3	−60	2	1.00	1	1	1.00	1			
4	−80	2	1.848	0.152	2	0.765	1.235			
5	−100	2	1.00	1	2	1.618	0.382	1	0.618	1.382
6	−120	2	1.932	0.068	2	1.414	0.586	2	0.518	1.482